IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims, AMEND claims, and ADD new claims, in accordance with the following:

1. (ORIGINAL) A control circuit having an error amplifier performing voltage control and controlling a direct-current to direct-current conversion, based on a pulse width modulation control using an output of said error amplifier, the error amplifier comprising:

a first input terminal inputting a voltage signal corresponding to an output voltage of a result of said direct-current to direct-current conversion;

a second input terminal inputting a predetermined reference voltage;

a third input terminal inputting a soft start signal when a power supply to said control circuit is turned on; and

an amplifier amplifying a difference between a voltage from said first input terminal and a voltage having a lower potential selected from voltage inputs from said second and third input terminals.

2. (CURRENTLY AMENDED) A control circuit having an error amplifier ~~for~~ performing voltage control and controlling a direct-current to direct-current conversion based on a pulse width modulation control using an output of said error amplifier, the error amplifier comprising:

a first input terminal inputting a voltage signal corresponding to an output voltage of a result of said direct-current to direct-current conversion;

a second input terminal inputting a predetermined reference voltage;

a third input terminal inputting a soft start signal when a power supply to said control circuit is turned on;

a comparator selecting a voltage having a lower potential among voltage inputs from said second and third input terminals; and

an amplifier amplifying a difference between a voltage from said first input terminal and an output voltage of said comparator.

3. (CURRENTLY AMENDED) A control circuit, comprising:

a first control circuit having a first error amplifier performing voltage control and controlling direct-current to direct-current conversion, based on a pulse width~~;~~ ~~a~~ modulation ~~controller~~ control using an output of said first error amplifier;

a second control circuit having a second error amplifier performing voltage control and controlling direct-current to direct-current conversion, based on a pulse width~~;~~ ~~a~~ modulation ~~controller~~ control using an output of said second error amplifier;

wherein each of said first and second error amplifiers further comprises:

a first input terminal inputting a voltage signal corresponding to an output voltage of a result of said direct-current to direct-current conversion,

a second input terminal inputting a predetermined reference voltage,

a third input terminal for inputting a soft start signal when a power supply to said control circuit is turned on,

an amplifier amplifying a difference between a voltage from said first input terminal and a voltage having a lower potential, selected from voltage inputs from said second and third input terminals, and

wherein a soft start signal is commonly supplied to said first and second error amplifiers.

4. (ORIGINAL) A control circuit, comprising:

a first control circuit having a first error amplifier performing voltage control and controlling a direct-current to direct-current conversion, based on a pulse width modulation control using an output of said first error amplifier;

a second control circuit having a second error amplifier for voltage control and controlling a direct-current to direct-current conversion, based on a pulse width modulation control using an output of said second error amplifier;

wherein a soft start signal is commonly supplied to said first and second error amplifiers and each of said first and second error amplifiers comprises:

a first input terminal inputting a voltage signal corresponding to an output voltage of a result of said direct-current to direct-current conversion, and

an amplifier amplifying a difference between a voltage from said first input terminal and a reference voltage gradually rising when the direct-current to direct-current conversion starts and becoming a constant value after a constant time.

5. (ORIGINAL) The control circuit as set forth in claim 1, wherein said soft start signal is supplied to said third input terminal of said error amplifier through a reference voltage circuit, the reference voltage circuit being comprised of a power supply unit and an FET.

6. (ORIGINAL) The control circuit as set forth in claim 2, wherein said soft start signal is supplied to said third input terminal of said error amplifier through a reference voltage circuit, the reference voltage circuit being comprised of a power supply unit and an FET.

7. (ORIGINAL) The control circuit as set forth in claim 5, wherein said power supply unit is a power supply unit controlling on/off of the control circuit, starts/stops of the operation by an external ON signal which controls on/off of the power supply to the control circuit.

8. (ORIGINAL) The control circuit as set forth in claim 6, wherein said power supply unit is a power supply unit controlling on/off of the control circuit, starts/stops of the operation by an external ON signal which controls on/off of the power supply to the control circuit.

9. (ORIGINAL) The control circuit as set forth in claim 7, wherein said power supply unit turns on switching circuits FET's simultaneously when the power supply unit makes the control circuit off-state.

10. (ORIGINAL) The control circuit as set forth in claim 1, further comprising a synchronous rectifying control circuit which outputs a signal controlling a synchronous rectifying transistor, based on a result of said direct-current to direct-current conversion.

11. (ORIGINAL) The control circuit as set forth in claim 2, further comprising a synchronous rectifying control circuit which outputs a signal controlling a synchronous rectifying transistor, based on a result of said direct-current to direct-current conversion.

12. (CURRENTLY AMENDED) The control circuit as set forth in claim 10, wherein said synchronous rectifying control circuit outputs said signal controlling said synchronous rectifying transistor, based on a result of said pulse width modulation control.

13. (CURRENTLY AMENDED) The control circuit as set forth in claim 11, wherein said synchronous rectifying control circuit outputs said signal for controlling said synchronous rectifying transistor based on a result of said pulse width modulation control.